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Chapter 1 Exercise Solutions. VLSI Test Principles and Architectures Ch. 1 - Introduction - P. 1/2. Chapter 1 Exercise Solutions. 1.1. There are 14 nodes in the circuit. Thus, there are  $14 \times 2 = 28$  single stuck-at faults. For multiple stuck-at fault, it has  $(2 + 1)14 - 1 = 4782968$  multiple stuck-at faults.

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$S_i = C_i + A_i + B_i$ ,  $C_{i+1} = C_i(A_i + B_i) + A_i B_i$ . VLSI Test Principles and Architectures Ch. 2 – Design for Testability – P. 3/12. 2.5 (Ad Hoc Technique) Fig. 7: An example of a combinational feedback loop in a combinational circuit. Figure 7 shows an example of a combinational feedback loop. In this example, when  $A = 1$ ,  $B = 0$ , and  $C = 1$ , the circuit acts as an oscillator, which prevents us from being able to predict a valid value at  $G$ .

## Chapter 2 Exercise Solutions 2.1 Testability Analysis

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